CLAIMS

I claim:

1. A central processing unit, comprising:

a plurality of functional units, each functional unit adapted to execute an instruction; and

a grouping logic circuit, including a number of pipeline stages and receiving, at each processor cycle, a group of instructions, said grouping logic circuit dispatching each of said instructions to be executed by one of said functional units.

2. A central processing unit as in Claim 1, wherein said grouping logic circuit checks data dependency among said group of instructions to determine whether said group of instructions can be dispatched simultaneously.

3. A central processing unit as in Claim 1, wherein said grouping logic circuit checks for resource contention within said group of instructions.

4. A central processing unit as in Claim 1, wherein said grouping logic circuit checks data dependency of an instruction group at one processor cycle and a group of instruction received in a previous processor cycle.

5. A central processing unit as in Claim 1, wherein the state of said central processing unit is represented in a register, said state including representation of destination registers of instructions in said group of instructions.

6. A central processing unit as in Claim 1, wherein all instruction in a group of instructions

received in a first processor cycle are dispatched prior to dispatching any instruction of a second group of instructions received at an processor cycle subsequent to said first processor cycle.

7. A central processing unit as in Claim 1, wherein said functional units include a pipelined functional unit capable of receiving an instruction every processor cycle and completing said instruction at a subsequent processor cycle.

8. A central processing unit as in Claim 1, wherein said functional units include a functional unit requiring multiple processor cycles to complete an instruction executed at said functional unit.

9. ~~A central processing unit as in Claim 1,~~ wherein said grouping logic circuit derives a state vector for a group of instructions received at a first processor cycle based on a number of state vectors derived for groups of instructions received in a number of processor cycles immediately preceding said first processor cycle, said number of processor cycles being ~~equal to said number of pipeline stages.~~